REMARKS/ARGUMENTS

1. Claims 1-36 are Patentable Over the Cited Art

The Examiner rejected claims 1-35 as anticipated (35 U.S.C. §102(b)) by Stotzer (EP1113356).. Applicants traverse.

Claims 1, 13, and 24 require: accessing a program comprising a plurality of instructions including at least one no operation (NOP) instruction; determining one instruction in the program preceding a determined NOP instruction whose movement forward to replace the determined NOP instruction will not result in data not being available when needed; and replacing the determined NOP instruction with the determined instruction preceding the determined NOP instruction.

The Examiner cited paras. 45-63 and 67 and associated examples of Stotzer as disclosing the claim requirement of determining one instruction in the program preceding a determined NOP instruction whose movement forward to replace the determined NOP instruction will not result in data not being available when needed. (OA4, pg. 3) Applicants traverse.

A below review of the cited paras. 45-63 and 67 reveals that they discuss the use of an operation code to specify a number of pseudo NOP delays to include in the code following the instruction including the NOP operation code. The below review reveals that the cited Stotzer does not disclose or mention the claim requirement of determining one instruction in the program preceding a determined NOP instruction whose movement forward to replace the determined NOP instruction will not result in data not being available when needed.

For instance, para. 44 mentions that an NOP operation may be encoded into or onto the instruction so that the NOP operation is issued in parallel with the instruction requiring the latency. Paras. 45 and 46 show an NOP field as an instruction operand specifying the number of times to insert pseudo NOP delay slots into the code, as discussed in paras. 47-50. Applicants submit that the cited operation code indicating a number of times to insert a pseudo NOP delay slot does not disclose or concern the claimed operation of determining one instruction in the program preceding a determined NOP instruction to move forward.

Other cited paragraphs are similarly deficient. Para. 48 discusses a branch instruction performing a relative branch with NOPs, a BNOP. The op code may be the first byte of the machine code. A constant specifies the number of NOP delay slots to insert. According to para.

52, the BNOP instructions may be predicated, and the predicate conditions control whether a branch is taken but do not control the insertion of delays. Other cited paragraphs provide further details on how the cited NOP and BNOP instruction operate. Paras. 53-54 mentions that if a BNOP instruction is used and the total number of NOP delays to insert exceeds a number, the NOP delay slots are only inserted when the predicate condition is false. Paras. 58-63 discuss further details on how BNOP instructions are predicate, and how the predicate condition controls whether the branch is taken, but does not effect the insertion of NOP delays.

The cited para. 67 also discusses the NOP field in a load instructions that defines the latency following the load instruction, and determining a latency following a branch instruction and inserting an NOP field into the branch instruction.

All the above cited paragraphs discuss an operation code to use with instructions to specify a number of pseudo NOP delay slots to insert following the instruction in which the NOP code is included. This does not disclose or mention the claim requirement of determining one instruction in the program preceding a determined NOP instruction whose movement forward to replace the determined NOP instruction will not result in data not being available when needed. In fact, the discussion in Stotzer differs and discusses how to include an NOP op code in an instruction, not how to determine instructions that may be moved forward to replace the NOP instruction.

Yet further the above discussion about using an op code field for an NOP instruction does not disclose or mention determining whether the movement forward of an instruction will not result in data not being available as claimed.

The Examiner cited para. 67 as disclosing the claim requirement of replacing the determined NOP instruction with the determined instruction preceding the determined NOP instruction. (OA4, pg. 3) Applicants traverse.

The cited para. 67 discusses the NOP field in a load instructions that defines the latency following the load instruction, and determining a latency following a branch instruction and inserting an NOP field into the branch instruction. Although the cited para. 67 mentions deleting the NOPs from the code, they are not removed but instead replaced by "inserting a NOP field into the delayed effect instructions:, or instructions for which the NOP delay is to follow. Thus, the cited para. 67 does not disclose that a NOP instruction is replaced by a determined instruction preceding the NOP whose movement forward will not result in data not being

available. Instead, the cited para. 67 discusses how the delay of an NOP may be coded into the instruction, which does not involve replacing the NOP instruction with a preceding instruction, just providing a different way to code the NOP delay slots.

Accordingly, claims 1, 13, and 24 are patentable over the cited art because the cited Stotzer does not disclose all the claim requirements.

Claims 2-12, 14-23 and 25-34 are patentable over the cited art because they depend from one of claims 1, 13, and 34. Further, the below discussed claims provide additional grounds of patentability over the cited art.

Claims 2, 14, and 25 depend from claims 1, 13, and 24, respectively, and further require deleting one NOP instruction in the program that is not needed to provide a processing delay to ensure the data is available to at least one dependent instruction without moving a non-NOP instruction.

The Examiner cited the above discussed para. 67 of Stotzer as disclosing these claim requirements (OA4, pg. 3) Applicants traverse.

As discussed, the cited Stotzer does not disclose deleting an NOP instruction not needed to provide a processing delay, but instead discusses how the number of NOP delays to add may be included in an NOP field or op code of the instruction.

Accordingly, claims 2, 14, and 25 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not disclosed in the cited Stotzer.

Claims 3, 15, and 26 depend from claims 1, 13, and 24, respectively, and further require deleting at least one instruction in the program that is not needed to provide the processing delay to ensure the data is available to at least one dependent instruction; and after deleting the at least one instruction, replacing at least one NOP instruction with one determined instruction whose movement forward to replace the determined NOP instruction will not result in data not being available when needed.

The Examiner cited the above discussed paragraphs of Stotzer as disclosing the claim requirement of after deleting the at least one instruction, replacing at least one NOP instruction with one determined instruction whose movement forward to replace the determined NOP instruction will not result in data not being available when needed. (OA4, pg. 4) Applicants traverse.

As discussed, the cited Stotzer discusses how a number of times to insert an NOP delay may be included in an NOP field of the delayed effect instruction to be followed by the delay. The cited Stotzer does not disclose that after deleting one instruction not needed to provide the processing delay, at least one NOP instruction is replaced with a determined preceding instruction. Instead, the cited Stotzer discusses how to code an NOP delay slot using an NOP field in the delayed effect instruction, and does not disclose moving one instruction forward to replace an NOP instruction after deleting at least one instruction not needed to provide the processing delay.

Accordingly, claims 3, 15, and 26 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not disclosed in the cited Stotzer.

Claims 6, 18, and 29 depend from claims 2, 14, and 25 and additionally require that deleting NOP instructions in the program further comprises accessing and processing each NOP instruction by: determining whether the accessed NOP instruction is needed to delay processing of one dependent instruction following the accessed NOP instruction to ensure that data is available to the dependent instruction accessing the data; and deleting the accessed NOP instruction in response to determining that the NOP instruction is not needed to ensure that data is available to the dependent instruction accessing the data..

The Examiner cited the above discussed para. 67 of Stotzer as disclosing these claim requirements. (OA4, pg. 5) Applicants traverse.

As discussed, the cited Stotzer discusses how an op code indicating number of times to insert a pseudo NOP delay slot may be included in an NOP field of the delayed effect instruction to be followed by the delay. Nowhere does this discussion of how to code an NOP delay in the instruction to be delayed disclose or mention the claim requirement of accessing and processing each NOP instruction by: determining whether the accessed NOP instruction is needed to delay processing of one dependent instruction following the accessed NOP instruction to ensure that data is available to the dependent instruction accessing the data. Instead, the cited Stotzer discusses how an op code in an instruction may specify to insert NOP delay slots into the code. There is no disclosure of determining whether an NOP instruction is needed to delay processing of one dependent instruction.

Accordingly, claims 6, 18, and 29 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not disclosed in the cited Stotzer.

Claims 8, 20, and 31 depend from claims 1, 13, and 24, respectively, and further require that the determining of one instruction in the program to move forward comprises determining one instruction whose movement forward to replace the determined NOP instruction will not result in data not being available to one dependent instruction following the NOP instruction.

The Examiner cited the above discussed Stotzer which discusses how to use an NOP field in an instruction to produce NOP delays following the instruction. (OA4, pg. 6)

Nowhere is there any disclosure or mention of the claim requirement of a determination of an instruction to move forward whose movement forward will not result in data not being available to one dependent instruction following the NOP instruction. The cited Stotzer does not disclose how to determine an instruction to move forward, but instead discusses how a delay may be introduced by including a value in an NOP field in the instruction to delay with a constant indicating the number of delay slots to insert.

Accordingly, claims 8, 20, and 31 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not taught in the cited Stotzer.

Claims 10, 22, and 33 depend from claims 8, 20, and 31 and further require deleting at least one NOP instruction not needed to ensure that data accessed by the dependent instruction is available to the dependent instruction, wherein the operations of replacing accessed NOP instructions with previous non-NOP instructions are performed after deleting NOP instructions not needed to ensure that data accessed by the dependent instruction is available.

The Examiner cited the above discussed Stotzer as disclosing the additional requirements of these claims. (OA4, pg. 7)) Applicants traverse.

As discussed, the Stotzer discussed how to use an op code in an NOP field in an instruction to introduce pseudo NOP delay slots following the instruction. Nowhere is there any disclosure or mention of the claim requirement of after deleting an NOP instruction, then replacing the NOP instruction with the determined instruction whose movement forward will not result in data not being available when needed.

Accordingly, claims 10, 22, and 33 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not taught or suggested in the cited Stotzer.

Claim 36 depends on claim 1and further recites that determining one instruction in the program preceding the determined NOP instruction whose movement forward to replace the determined NOP instruction will not result in data not being available when needed comprises determining whether the instruction to move forward causes the data needed by one dependent instruction to be written in fewer cycles such that the number of cycles between a writing instruction and the dependent instruction are not sufficient to guarantee that the written data will be available to the dependent instruction.

The Examiner cited the above discussed Stotzer as disclosing the requirements of claim 36. (OA4, pgs. 7-8) Applicants traverse.

As discussed, the cited Stotzer discusses how to use an NOP field in an instruction to specify to insert a number of delay slots. Nowhere does the cited Stotzer disclose or mention determining an instruction in the program to move forward preceding the NOP instruction to replace by determining whether the instruction to move forward causes the data needed by one dependent instruction to be written in fewer cycles such that the number of cycles between a writing instruction and the dependent instruction are not sufficient to guarantee that the written data will be available to the dependent instruction. There is no mention in the cited Stotzer of moving one instruction forward to replace an NOP instruction and making the claimed determination when deciding whether to move the instruction forward.

Accordingly, claim 36 provides additional grounds of patentability over the cited art because the additional requirements of these claims are not taught or suggested in the cited Stotzer.

Conclusion

For all the above reasons, Applicant submits that the pending claims 1-36 are patentable. Should any additional fees be required beyond those paid, please charge Deposit Account No. 50-0585.

The attorney of record invites the Examiner to contact him at (310) 553-7977 if the Examiner believes such contact would advance the prosecution of the case.

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